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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/802,590	03/17/2004	Greg Starr	A1346	3874

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EXAMINER	
YOUNG, BRIAN K	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 10/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/802,590	STARR ET AL.	
	Examiner	Art Unit	
	Brian Young	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 11* is/are rejected.

7)☒ Claim(s) *2-10 and 12-20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/17/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1 and 11 are rejected under 35 U.S.C. 102(b) as being anticipated by Soneda.

Soneda discloses an apparatus for sensing an electric charge appearing on at least one bit line of a memory cell comprises a pair of P-channel MOS (Metal Oxide Semiconductor) transistors whose sources are commonly connected, a pair of N-channel MOS (Metal Oxide Semiconductor) transistors whose sources are commonly connected, both pairs of the PMOS and NMOS transistors carrying out latch operations according to control signals supplied to their sources to sense the electric charge appearing on either a first or second bit line. In at least one of the pairs of PMOS and NMOS transistors, the gate of each MOS transistor is connected to either the first or second bit line via a capacitor, a first switching element is disposed between the drain of each MOS transistor and gate thereof, and a second switching element is disposed between the drain of each MOS transistor and a junction to either the first or second bit line. When control voltages applied to both sources of the PMOS transistors and NMOS transistors are changed and the switching elements are switched over during a precharge interval and sensing operation interval, the capacitors store voltages according to the respective threshold voltages of the PMOS and NMOS transistors ***so that divergence in the threshold voltages can be compensated for.***

The pair of CMOS transistors in the memory device constitutes the sensing amplifier. The sensing amplifier according to the present invention can assure an accurate sensing operation without reduction of sensitivity for the electric charge on the bit line due to the divergence in the threshold voltages of the respective transistors. Even when

the circuit elements constituting such a memory device as described above are miniaturized, the sensing amplifier according to the present invention can have a high sensitivity for sensing the electric charge appearing on the information bit line. Since the sensing amplifier according to the present invention can assure the sensing operation even when a capacitance of the capacitor incorporated in each memory cell is reduced due to the miniaturization of the IC memory device, high integrations of memory devices can be achieved in practice. Furthermore, since the sensing amplifier according to the present invention can completely compensate the MOS transistors for the divergence in the threshold voltages of the transistors, the yield of manufacturing memory devices can be improved and the accurate sensing operation can be ensured for a long time without suffering from the influences of the *aging* effects on the sensing amplifier.
As shown in FIG. 5, the capacitors C.sub.1 and C.sub.2 and first, second, third, and fourth switching elements S.sub.11, S.sub.21, 2.sub.12, and S.sub.22 are connected to the pair of PMOS transistors.

The sensing amplifier in the second preferred embodiment includes the pair of PMOS transistors whose sources are commonly connected and the pair of NMOS transistors whose sources are commonly connected. The pair of PMOS transistors includes the two PMOS transistors PM.sub.1 and PM.sub.2. The pair of NMOS transistors includes the two NMOS transistors. NM.sub.1 and NM.sub.2.

In the sensing amplifier of the second preferred embodiment, the control signal .phi..sub.SN whose level is changed to zero level with the constant time difference .DELTA.t from the control signal .phi.SP to be described later is supplied to the sources of the NMOS transistors NM.sub.1 and NM.sub.2. The drain of the NMOS transistor

NM.sub.1 is connected to the first bit line BL1. The drain of the NMOS transistor MN.sub.2 is connected to the second bit line BL2. The gate of the NMOS transistor NM.sub.1 is connected to the second bit line BL2.

The control voltage .phi..sub.SP is supplied to the sources of the PMOS transistors PM.sub.1 and PM.sub.2 in the pair of PMOS transistors which are compensated for the divergence of .DELTA.V.sub.th.

One end of the first switching element S.sub.11 and one end of the second switching element are connected to the drain of the PMOS transistor PM.sub.1. The other end of the first switching element S.sub.11 is connected to the gate of the PMOS transistor PM.sub.1. In addition, the other end of the second switching element S.sub.12 is connected to the first bit line BL1. The first and second switching elements S.sub.11 and S.sub.12 are controlled by means of the control signals .phi..sub.1 and .phi..sub.2. On the other hand, one end of the third switching element S.sub.21 and one end of the fourth switching element S.sub.22 are connected to the drain of the PMOS transistor PM.sub.2. The other end of the third switching element S.sub.21 is connected to the second bit line BL2. These third and fourth switching elements S.sub.21 and S.sub.22 are controlled by means of the control signals .phi..sub.1 and .phi..sub.2, respectively, in the same way as the first and second switching elements S.sub.11 and S.sub.12. Each gate of the PMOS transistors PM.sub.1 and PM.sub.2 constituting the pair of PMOS transistors of the sensing amplifier in the second preferred embodiment is

coupled to the corresponding capacitor C.sub.1 and C.sub.2. In detail, the gate of the PMOS transistor PM.sub.1 is connected to the other end of the first switching element S.sub.11 and to one end of the capacitor C.sub.1. The other end of the capacitor C.sub.1 is connected to the second bit line BL2. On the other hand, the gate of the PMOS transistor PM.sub.2 is connected to the other end of the first switching element S.sub.21 and to one end of the capacitor C.sub.2. The other end of the capacitor C.sub.2 is connected to the first bit line BL1. These capacitors C.sub.1 and C.sub.2 can serve to ***compensate*** the PMOS transistors for the divergence of .DELTA.V.sub.th in the threshold voltages of the pair of PMOS transistors.

3. Claims 2-10 and 12-20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian Young whose telephone number is 571-272-1816. The examiner can normally be reached on Mon-Fri 7:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mike Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Brian Young
Primary Examiner
Art Unit 2819

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